

- 1 1. A silicon controlled rectifier formed on a substrate comprising:
2 a first well region lightly doped with impurities of a first conductivity type
3 formed on said substrate;
4 a second well region formed within said first well region and lightly doped
5 with impurities of a second conductivity type;
6 a first diffusion region formed within said second well and heavily doped
7 with the impurities of the first conductivity type;
8 a second diffusion region formed within said first well region at a second
9 distance from the first diffusion region and heavily doped with
10 impurities of the second conductivity type; and
11 a heavily doped polycrystalline layer formed at the surface of said
12 substrate and placed between the s and astride a junction of the first
13 well region and the second well region to form a bounding component
14 to prevent silicide formation at junctions of the first diffusion region and
15 the second well region, the first well region and the second region, and
16 the second diffusion region and the first well region during fabrication
17 of said silicon controlled rectifier.
- 1 2. The silicon controlled rectifier of claim 1 wherein said heavily doped
2 polycrystalline layer permits a series resistance of said silicon controlled rectifier
3 to be smaller for a more efficient operation.

- 1 3. The silicon controlled rectifier of claim 1 wherein the heavily doped polycrystalline
2 layer is connected to bias said heavily doped polycrystalline silicon layer such
3 that salicide shorting is prevented said first and second diffusion regions and
4 preventing of accidental formation of an inversion region under said heavily
5 doped polycrystalline layer.
- 1 4. The silicon controlled rectifier of claim 3 wherein said heavily doped
2 polycrystalline silicon layer is connected to the second diffusion region.
- 1 5. The silicon controlled rectifier of claim 1 wherein the first diffusion region is linked
2 to a voltage source which provides a relatively large voltage which when said
3 relatively large voltage exceeds said snapback voltage, said silicon controlled
4 rectifier conducts.
- 1 6. The silicon controlled rectifier of claim 4 wherein the first well region, the second
2 well region, said highly doped polycrystalline silicon layer, and the second
3 diffusion are power supply connection.
- 1 7. The silicon controlled rectifier of claim 6 wherein a first parasitic resistance
2 formed within said first well region and a second parasitic resistance formed
3 within said second well region act to bias a first and second gate of said silicon
4 controlled rectifier to turn-on said silicon controlled rectifier.
- 1 8. An ESD protection circuit formed at an input/output of an integrated circuit to
2 protect said integrated circuit from damage caused by an ESD event, said ESD
3 protection circuit comprising:

4 a polycrystalline silicon bounded SCR connected between a signal
5 input/output interface of said integrated circuit and a power supply
6 connection of said integrated circuit, said polycrystalline silicon
7 bounded SCR comprising:

8 a first well region lightly doped with impurities of a first conductivity
9 type formed on said substrate and connected to said power supply
10 connection,

11 a second well region formed within said first well region and lightly
12 doped with impurities of a second conductivity type,

13 a first diffusion region formed within said second well, heavily doped
14 with the impurities of the first conductivity type, and connected to
15 said signal input/output interface,

16 a second diffusion region formed within said first well region at a
17 second distance from the first diffusion region, heavily doped with
18 impurities of the second conductivity type, and connected to said
19 power supply connection, and

20 a first heavily doped polycrystalline layer formed at the surface of said
21 substrate and placed between the first and second diffusion regions
22 and astride a junction of the first well region and the second well
23 region to form a bounding component to prevent silicide formation
24 at junctions of the first diffusion region and the second well region,

25 the first well region and the second region, and the second diffusion
26 region and the first well region during fabrication of said silicon
27 controlled rectifier; and

28 a biasing circuit connected to said polycrystalline silicon bounded SCR
29 to bias said polycrystalline silicon bounded SCR to turn on more
30 rapidly during said ESD event.

1 9. The ESD protection circuit of claim 8 further comprising at least one diode
2 formed on said substrate and connected between said signal input/output
3 interface and an anode connection of said polycrystalline silicon bounded SCR to
4 increase a holding voltage for said polycrystalline silicon bounded SCR when
5 said polycrystalline silicon bounded SCR is turned on.

1 10. The ESD protection circuit of claim 8 wherein said biasing circuit comprises:

2 a polycrystalline silicon bounded diode connected from the signal
3 input/output interface, said polycrystalline silicon bounded diode
4 comprising:

5 the first diffusion region,

6 the second well region, and

7 a second heavily doped polycrystalline layer formed at the
8 surface of said substrate and placed adjacent to the first
9 diffusion region and astride a junction of the second well

10 region and first diffusion region to form a bounding
11 component to prevent silicide formation at said junction of
12 the first diffusion region and the second well region during
13 fabrication of said polycrystalline silicon bounded diode;
14 wherein said junction of the first diffusion region and the second
15 well region forms said polycrystalline bounded diode; and
16 a first resistance formed of material of the second well from a first gate of
17 said polycrystalline silicon bounded SCR to a third diffusion region
18 formed within said second well, heavily doped with the impurities of the
19 second conductivity type, and connected to said power supply
20 connection to provide a low resistance path to said second well from
21 said power supply connection.

1 11. The ESD protection circuit of claim 10 wherein said biasing circuit: further
2 comprises:

3 a second resistance formed material of the second well from said first gate
4 to said first diffusion region.

1 12. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

2 a first resistor connected from the signal input/output interface to the
3 first gate of said polycrystalline silicon bounded SCR; and

4 a first capacitor connected from the first gate of the polycrystalline
5 silicon bounded SCR to said power supply connection;
6 wherein upon said ESD event, a top plate of said capacitor connected
7 to said gate of the polycrystalline bounded SCR is a virtual ground
8 and said polycrystalline silicon bounded SCR is activated.

1 13. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

2 a plurality of serially connected diodes, where a first diode of said plurality
3 of serially connected diodes is connected to the signal input/output
4 interface and a last diode of said plurality of serially connected diodes
5 is connected to a second gate of said polycrystalline silicon bounded
6 SCR; and

7 a second resistor connected from the second gate and the last diode of
8 the plurality of serially connected diodes to the power supply
9 connection;

10 wherein an ESD event causes a current to flow through said plurality of
11 serially connected diodes and said second resistor to trigger the
12 polycrystalline silicon bounded SCR to turn on.

1 14. The ESD protection circuit of claim 8 wherein said biasing circuit: comprises:

2 a resistor/capacitor biasing circuit comprising:

3 a first resistor connected from the signal input/output interface to
4 the first gate of said polycrystalline silicon bounded SCR,
5 and

6 a first capacitor connected from the first gate of the
7 polycrystalline silicon bounded SCR to said power supply
8 connection,

9 wherein upon occurrence of said ESD event, a top plate of said
10 capacitor connected to said gate of the polycrystalline
11 bounded SCR virtually connected to said power supply
12 connection and said polycrystalline silicon bounded SCR is
13 activated;

14 a diode triggering biasing circuit comprising:

15 a plurality of serially connected diodes, where a first diode of said
16 plurality of serially connected diodes is connected to the signal
17 input/output interface and a last diode of said plurality of serially
18 connected diodes is connected to a second gate of said
19 polycrystalline silicon bounded SCR, and

20 a second resistor connected from the second gate and the last diode of
21 the plurality of serially connected diodes to the power supply
22 connection,

23 wherein an ESD event causes a current to flow through said plurality of
24 serially connected diodes and said second resistor to trigger the
25 polycrystalline silicon bounded SCR to turn on.

1 15. The ESD protection circuit of claim 8 wherein said biasing circuit comprises:

2 a resistor/capacitor biasing circuit comprising:

3 a second resistor connected from the signal input/output
4 interface, said second resistor including a first metal oxide
5 semiconductor transistor of a first conductivity type with a
6 source connected to the signal input/output interface and a
7 gate connected so as to have a voltage level approximately
8 equal the power supply connection of said integrated circuit,
9 and

10 a second capacitor connected between the second resistor and
11 said power supply connection, said second capacitor
12 including a second metal oxide semiconductor transistor with
13 a drain and source connected to a drain of said second
14 metal oxide semiconductor transistor and a gate connected
15 to said power supply connection; and

16 an SCR triggering circuit with an input connected to a junction of said
17 second resistor and said second capacitor, said SCR trigger circuit
18 comprising:

19 a plurality of serially connected inverter circuits,
20 wherein an input to a first inverter of the plurality of serially
21 connected inverter circuits is connected to the junction of
22 said second resistor and said second capacitor,
23 wherein an in phase output that provides a signal that is in
24 phase with said input to said first inverter is connected to the
25 first gate of said polycrystalline silicon bounded SCR,
26 wherein an out-of-phase output that provides a signal that is out
27 of phase with said input to said first inverter is connected to
28 the second gate of said polycrystalline silicon bounded SCR;
29 wherein upon occurrence of said ESD event, a top plate of said second
30 capacitor is virtually connected to said power supply connection to
31 cause said plurality of serially connected inverters to activate with a
32 sharp transition and clearly defined windown to trigger the
33 polycrystalline silicon bounded SCR to turn on.

1 16. The ESD protection circuit of claim 15 further comprising:

2 a diode connected between the polycrystalline silicon bounded SCR and
3 said signal input/output interface of said integrated circuit to increase a
4 holding voltage of said polycrystalline silicon bounded SCR.

1 17. The ESD protection circuit of claim 15 wherein said biasing circuit further
2 comprises:

3 a diode connected between said first inverter said plurality of serially
4 connected inverters and said signal input/output interface of said
5 integrated circuit to avoid unintended triggering of said ESD protection
6 circuit.

1 18. The ESD protection circuit of claim 8 wherein said biasing circuit comprises:

2 a resistor/capacitor biasing circuit comprising:

3 a third resistor connected from the signal input/output interface,
4 said third resistor including a second metal oxide
5 semiconductor transistor of the first conductivity type with a
6 source connected to the signal input/output interface and a
7 gate connected so as to have a voltage level approximately
8 equal the power supply connection of said integrated circuit,
9 and

10 a third capacitor connected between the third resistor and said
11 power supply connection, said third capacitor including a
12 fourth metal oxide semiconductor transistor with a drain and
13 source connected to a drain of said third metal oxide
14 semiconductor transistor; and

15 an SCR triggering circuit with an input connected to a junction of said third
16 resistor and said third capacitor, said SCR trigger circuit comprising:
17 an inverter including:
18 an input connected to the junction of said second resistor and
19 said second capacitor,
20 a weak feedback pull-up metal oxide semiconductor transistor to
21 provide a sharp transition and a clearly defined window
22 when said polycrystalline silicon bounded SCR is turned on,
23 an in phase output that provides a signal that is in phase with
24 said input to said inverter is connected to the first gate of
25 said polycrystalline silicon bounded SCR, and
26 an out-of-phase output that provides a signal that is out of
27 phase with said input to said inverter is connected to the
28 second gate of said polycrystalline silicon bounded SCR;
29 wherein upon occurrence of said ESD event, a top plate of said second
30 capacitor is virtually connected to said power supply connection to
31 cause said inverter to activate with the sharp transition and the
32 clearly defined window to trigger the polycrystalline silicon bounded
33 SCR to turn on.

1 19. The ESD protection circuit of claim 15 further comprising:

2 a diode connected between the polycrystalline silicon bounded SCR and
3 said signal input/output interface of said integrated circuit to increase a
4 holding voltage of said polycrystalline silicon bounded SCR.

1 20. The ESD protection circuit of claim 15 wherein said biasing circuit further
2 comprises:

3 a diode connected between said inverter and said signal input/output
4 interface of said integrated circuit to avoid unintended triggering of said
5 ESD protection circuit.

1 21. The ESD protection circuit of claim 8 wherein said heavily doped polycrystalline
2 layer of the polycrystalline silicon bounded SCR permits a series resistance of
3 said polycrystalline silicon bounded SCR to be smaller for a more efficient
4 operation.

1 22. The ESD protection circuit of claim 8 wherein the heavily doped polycrystalline
2 layer is connected to bias said heavily doped polycrystalline silicon layer such
3 that silicide shorting is prevented said first and second diffusion regions and
4 preventing of accidental formation of an inversion region under said heavily
5 doped polycrystalline layer.

1 23. The ESD protection circuit of claim 22 wherein said heavily doped polycrystalline
2 silicon layer is connected to the second diffusion region.

1 24. The ESD protection circuit of claim 22 wherein the first diffusion region is linked
2 to a voltage source which provides a relatively large voltage during said ESD
3 event which when said relatively large voltage exceeds said snapback voltage,
4 said polycrystalline silicon bounded SCR conducts.

1 25. The ESD protection circuit of claim 23 wherein the first well region, the second
2 well region, said highly doped polycrystalline silicon layer, and the second
3 diffusion are power supply connection .

1 26. The ESD protection circuit of claim 25 wherein a first parasitic resistance formed
2 within said first well region and a second parasitic resistance formed within said
3 second well region act to bias a first and second gate of said silicon controlled
4 rectifier to turn-on said polycrystalline silicon bounded SCR.

1 27. A method for fabricating a silicon controlled rectifier on a substrate comprising
2 the steps of:


3 forming a first well region lightly doped with impurities of a first conductivity
4 type on a surface of said substrate;

5 forming a second well region within said first well region by lightly doping
6 said second well region with impurities of a second conductivity type,
7 said impurities of the second conductivity type having a polarity
8 opposite the impurities of the first conductivity type;

9 forming a first diffusion region within said second well by heavily doping
10 said first diffusion region with the impurities of the first conductivity
11 type;
12 forming a second diffusion region within said first well region at a second
13 distance from the first diffusion region by heavily doping said second
14 diffusion region with impurities of the second conductivity type; and
15 forming a heavily doped polycrystalline layer at the surface of said
16 substrate and between the first and second diffusion regions and
17 astride a junction of the first well region and the second well region to
18 form a bounding component to prevent silicide formation at junctions of
19 the first diffusion region and the second well region, the first well region
20 and the second region, and the second diffusion region and the first
21 well region during fabrication of said silicon controlled rectifier.

1 28. The method of claim 27 wherein said heavily doped polycrystalline layer permits
2 a series resistance of said silicon controlled rectifier to be smaller for a more
3 efficient operation.

1 29. The method of claim 27 further comprises the step of connecting the heavily
2 doped polycrystalline layer to bias said heavily doped polycrystalline silicon layer
3 such that silicide shorting is prevented said first and second diffusion regions and
4 preventing of accidental formation of an inversion region under said heavily
5 doped polycrystalline layer.

- 1 30. The method of claim 29 further comprising the step of connecting said heavily
2 doped polycrystalline silicon layer to the second diffusion region.
- 1 31. The method of claim 27 further comprising the step of linking the first diffusion
2 region to a voltage source which provides a relatively large voltage which when
3 said relatively large voltage exceeds said snapback voltage, said silicon
4 controlled rectifier conducts.
- 1 32. The method of claim 30 further comprising the step of linking the first well region,
2 the second well region, said highly doped polycrystalline silicon layer, and the
3 second diffusion to a return of the voltage source.
- 1 33. The method of claim 32 wherein a first parasitic resistance formed within said
2 first well region and a second parasitic resistance formed within said second well
3 region act to bias a first and second gate of said silicon controlled rectifier to turn-
4 on said silicon controlled rectifier.
- 1 34. A method for forming an ESD protection circuit formed at an input/output 
2 interface of an integrated circuit formed on a substrate to protect said integrated
3 circuit from damage caused by an ESD event, said ESD protection circuit
4 comprising:
- 5 forming a polycrystalline silicon bounded SCR on a surface of said
6 substrate by the steps of :

7 forming a first well region lightly doped with impurities of a first
8 conductivity type on a surface of said substrate,

9 forming a second well region within said first well region by lightly
10 doping said second well region with impurities of a second
11 conductivity type, said impurities of the second conductivity type
12 having a polarity opposite from the impurities of the first
13 conductivity type,

14 forming a first diffusion region within said second well by heavily
15 doping said first diffusion region with the impurities of the first
16 conductivity type,

17 forming a second diffusion region within said first well region at a
18 second distance from the first diffusion region by heavily doping
19 said second diffusion region with impurities of the second
20 conductivity type, and

21 forming a heavily doped polycrystalline layer at the surface of said
22 substrate and between the first and second diffusion regions and
23 astride a junction of the first well region and the second well region
24 to form a bounding component to prevent silicide formation at
25 junctions of the first diffusion region and the second well region, the
26 first well region and the second region, and the second diffusion

27 region and the first well region during fabrication of said silicon
28 controlled rectifier;

29 connecting said polycrystalline silicon bounded SCR between a signal
30 input/output interface of said integrated circuit and a power supply
31 connection of said integrated circuit;

32 forming a biasing circuit; and

33 connecting said biasing circuit to said polycrystalline silicon bounded SCR
34 to bias said polycrystalline silicon bounded SCR to turn on more
35 rapidly during said ESD event.

1 35. The method of claim 34 further comprising the steps of:

2 forming at least one diode on said substrate; and

3 connecting said diode between said signal input/output interface and an
4 anode connection of said polycrystalline silicon bounded SCR to
5 increase a holding voltage for said polycrystalline silicon bounded SCR
6 when said polycrystalline silicon bounded SCR is turned on.

1 36. The method of claim 34 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a polycrystalline silicon bounded diode said polycrystalline silicon
4 bounded diode by the steps of:

5 forming the first diffusion region,

6 forming the second well region, and

7 forming a second heavily doped polycrystalline layer at the

8 surface of said substrate and placed adjacent to the first

9 diffusion region and astride a junction of the second well

10 region and first diffusion region to form a bounding

11 component to prevent silicide formation at said junction of

12 the first diffusion region and the second well region during

13 fabrication of said polycrystalline silicon bounded diode;

14 wherein said junction of the first diffusion region and the second

15 well region forms said polycrystalline bounded diode; and

16 connecting said polycrystalline silicon bounded diode to the signal

17 input/output interface,

18 forming a third diffusion region within said second well by heavily doping

19 said third diffusion region with the impurities of the second conductivity

20 type,

21 forming a first resistance of material of the second well from a first gate of

22 said polycrystalline silicon bounded SCR to said third diffusion region,

23 and

24 connecting said third diffusion region to said power supply connection to
25 provide a low resistance path to said second well from said power
26 supply connection.

1 37. The method of claim 36 wherein forming said biasing circuit further comprises the
2 steps of:

3 forming a second resistance of the material of the second well from said
4 first gate to said first diffusion region.

1 38. The method of claim 34 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a first resistor from the signal input/output interface to the first
4 gate of said polycrystalline silicon bounded SCR; and

5 forming a first capacitor from the first gate of the polycrystalline silicon
6 bounded SCR to said power supply connection;

7 wherein upon said ESD event, a top plate of said capacitor connected
8 to said gate of the polycrystalline bounded SCR virtually connected
9 to said power supply connection and said polycrystalline silicon
10 bounded SCR is activated.

1 39. The method of claim 34 wherein said biasing circuit: comprises the steps of:

2 forming a plurality of serially connected diodes;

3 connecting a first diode of said plurality of serially connected diodes to the
4 signal input/output interface;
5 connecting a last diode of said plurality of serially connected diodes to a
6 second gate of said polycrystalline silicon bounded SCR; and
7 forming a second resistor from the second gate and the last diode of the
8 plurality of serially connected diodes to the power supply connection;
9 wherein an ESD event causes a current to flow through said plurality of
10 serially connected diodes and said second resistor to trigger the
11 polycrystalline silicon bounded SCR to turn on.

1 40. The method of claim 34 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a resistor/capacitor biasing circuit by the steps of:

4 forming a first resistor from the signal input/output interface to
5 the first gate of said polycrystalline silicon bounded SCR,
6 and

7 forming a first capacitor from the first gate of the polycrystalline
8 silicon bounded SCR to said power supply connection,

9 wherein upon said ESD event, a top plate of said capacitor
10 connected to said gate of the polycrystalline bounded SCR

virtually connected to said power supply connection and said polycrystalline silicon bounded SCR is activated.

13 forming a diode triggering biasing circuit by the steps of:

14 forming a plurality of serially connected diodes;

15 connecting a first diode of said plurality of serially connected diodes to
16 the signal input/output interface,

connecting a last diode of said plurality of serially connected diodes to
a second gate of said polycrystalline silicon bounded SCR, and

19 forming a second resistor from the second gate and the last diode of
20 the plurality of serially connected diodes to the power supply
21 connection.

22 wherein an ESD event causes a current to flow through said plurality of
23 serially connected diodes and said second resistor to trigger the
24 polycrystalline silicon bounded SCR to turn on.

1 41. The method of forming the ESD protection circuit of claim 34 wherein forming
2 said biasing circuit comprises the steps of:

3 creating a resistor/capacitor biasing circuit by the steps of:

4 forming a third resistor by the steps of:

5 creating a second metal oxide semiconductor transistor of
6 the first conductivity type,

7 connecting a source of said second metal oxide
8 semiconductor transistor to the signal input/output
9 interface, and

10 connecting a gate of said second metal oxide semiconductor
11 transistor so as to have a voltage level approximately
12 equal the power supply connection of said integrated
13 circuit, and

14 forming a third capacitor by the steps of;

15 creating a fourth metal oxide semiconductor transistor,

16 connecting a drain and a source of said fourth metal oxide
17 semiconductor transistor to a drain of said third metal
18 oxide semiconductor transistor and, and

19 connecting a gate of said fourth metal oxide semiconductor
20 to said power supply connection; and

21 forming an SCR triggering circuit by the steps of:

22 forming an inverter,

23 connecting an input of said inverter to the junction of said second
24 resistor and said second capacitor,
25 forming a weak feedback pull-up metal oxide semiconductor transistor
26 within said inverter to provide a sharp transition and a clearly
27 defined window when said polycrystalline silicon bounded SCR is
28 turned on,
29 connecting an in phase output of said inverter to the first gate of said
30 polycrystalline silicon bounded SCR, said in phase output providing
31 a signal that is in phase with said input to said inverter and
32 connecting an out-of-phase output of said inverter to the second gate
33 of said polycrystalline silicon bounded SCR, said inverter providing
34 a signal that is out of phase with said input to said inverter; and
35 connecting an input of the SCR triggering circuit to a junction of said third
36 resistor and said third capacitor,
37 wherein upon occurrence of said ESD event, a top plate of said second
38 capacitor is virtually connected to said power supply connection to
39 cause said inverter to activate with a sharp transition and clearly
40 defined window to trigger the polycrystalline silicon bounded SCR to
41 turn on.

1 42. The method of forming the ESD protection circuit of claim 41 further comprising
2 the steps of :

3 connecting a diode between the polycrystalline silicon bounded SCR and
4 said signal input/output interface of said integrated circuit to increase a
5 holding voltage of said polycrystalline silicon bounded SCR.

1 43. The method of forming the ESD protection circuit of claim 41 wherein forming
2 said biasing circuit further comprises the step of :

3 connecting a diode between said inverter and said signal input/output
4 interface of said integrated circuit to avoid unintended triggering of said
5 ESD protection circuit.

1 44. The method of forming the ESD protection circuit of claim 34 wherein forming
2 said biasing circuit comprises the steps of :

3 creating a resistor/capacitor biasing circuit by the steps of:

4 forming a third resistor by the steps of:

5 creating a second metal oxide semiconductor transistor of
6 the first conductivity type,

7 connecting a source of said second metal oxide
8 semiconductor transistor to the signal input/output
9 interface, and

10 connecting a gate of said second metal oxide semiconductor
11 transistor so as to have a voltage level approximately
12 equal the power supply connection of said integrated
13 circuit, and

14 forming a third capacitor by the steps of,

15 creating a fourth metal oxide semiconductor transistor,

16 connecting a drain and a source of said fourth metal oxide
17 semiconductor transistor to a drain of said third metal
18 oxide semiconductor transistor and, and

19 connecting a gate of said fourth metal oxide semiconductor
20 to said power supply connection; and

21 forming an SCR triggering circuit said SCR trigger circuit comprising:

22 an inverter including:

23 an input connected to the junction of said second resistor and
24 said second capacitor,

25 a weak feedback pull-up metal oxide semiconductor transistor to
26 provide a sharp transition and a clearly defined window
27 when said polycrystalline silicon bounded SCR is turned on,

28 an in phase output that provides a signal that is in phase with
29 said input to said inverter is connected to the first gate of
30 said polycrystalline silicon bounded SCR, and

31 an out-of-phase output that provides a signal that is out of
32 phase with said input to said inverter is connected to the
33 second gate of said polycrystalline silicon bounded SCR;
34 and

35 connecting an input of said SCR triggering circuit to a junction of said third
36 resistor and said third capacitor;

37 wherein upon occurrence of said ESD event, a top plate of said second
38 capacitor is virtually connected to said power supply connection to
39 cause said inverter to activate with a sharp transition and a clearly
40 defined window to trigger the polycrystalline silicon bounded SCR to
41 turn on.

1 45. The method of forming the ESD protection circuit of claim 41 further comprising
2 the step of:

3 connecting a diode between the polycrystalline silicon bounded SCR and
4 said signal input/output interface of said integrated circuit to increase a
5 holding voltage of said polycrystalline silicon bounded SCR.

- 1 46. The method of forming the ESD protection circuit of claim 41 wherein forming
2 said biasing circuit further comprises the step of:
- 3 connecting a diode between said inverter and said signal input/output
4 interface of said integrated circuit to avoid unintended triggering of said
5 ESD protection circuit.
- 1 47. The method of claim 34 wherein said heavily doped polycrystalline layer of the
2 polycrystalline silicon bounded SCR permits a series resistance of said
3 polycrystalline silicon bounded SCR to be smaller for a more efficient operation.
- 1 48. The method of claim 34 further comprising the step of connecting the heavily
2 doped polycrystalline layer to bias said heavily doped polycrystalline silicon layer
3 such that silicide shorting is prevented said first and second diffusion regions and
4 preventing of accidental formation of an inversion region under said heavily
5 doped polycrystalline layer.
- 1 49. The method of claim 48 further comprising the step of connecting said heavily
2 doped polycrystalline silicon layer to the second diffusion region.
- 1 50. The method of claim 48 further comprising the step of linking the first diffusion
2 region to a voltage source which provides a relatively large voltage during said
3 ESD event which when said relatively large voltage exceeds said snapback
4 voltage, said polycrystalline silicon bounded SCR conducts.

1 51. The method of claim 49 further comprising the step of linking the first well region,
2 the second well region, said highly doped polycrystalline silicon layer, and the
3 second diffusion to a return of the voltage source.

1 52. The method of claim 51 further comprising the steps of:

2 forming a first parasitic resistance formed within said first well region and a
3 second parasitic resistance within said second well region act to bias a
4 first and second gate of said silicon controlled rectifier to turn-on said
5 polycrystalline silicon bounded SCR.

1 53. An ESD protection circuit formed at an input/output of an integrated circuit to
2 protect said integrated circuit from damage caused by an ESD event, said ESD
3 protection circuit comprising:

4 a shallow trench isolation bounded SCR connected between a signal
5 input/output interface of said integrated circuit and a power supply
6 connection of said integrated circuit; and

7 a biasing circuit connected to said shallow trench isolation bounded
8 SCR to bias said shallow trench isolation bounded SCR to turn on
9 more rapidly during said ESD event.

1 54. The ESD protection circuit of claim 53 further comprising at least one diode
2 formed on said substrate and connected between said signal input/output
3 interface and an anode connection of said shallow trench isolation bounded SCR

4 to increase a holding voltage for said shallow trench isolation bounded SCR
5 when said shallow trench isolation bounded SCR is turned on.

1 55. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

2 a shallow trench isolation bounded diode connected from the signal
3 input/output interface; and

4 a first resistance formed of material of the second well from a first gate of
5 said shallow trench isolation bounded SCR to a third diffusion region
6 formed within said second well, heavily doped with the impurities of the
7 second conductivity type, and connected to said power supply
8 connection to provide a low resistance path to said second well from
9 said power supply connection.

1 56. The ESD protection circuit of claim 55 wherein said biasing circuit: further
2 comprises:

3 a second resistance formed material of the second well from said first gate
4 to said first diffusion region.

1 57. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

2 a first resistor connected from the signal input/output interface to the
3 first gate of said shallow trench isolation bounded SCR; and

4 a first capacitor connected from the first gate of the shallow trench
5 isolation bounded SCR to said power supply connection;
6 wherein upon said ESD event, a top plate of said capacitor connected
7 to said gate of the shallow trench isolation bounded virtually
8 connected to said power supply connection and said shallow trench
9 isolation bounded SCR is activated.

1 58. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

2 a plurality of serially connected diodes, where a first diode of said plurality
3 of serially connected diodes is connected to the signal input/output
4 interface and a last diode of said plurality of serially connected diodes
5 is connected to a second gate of said shallow trench isolation bounded
6 SCR; and

7 a second resistor connected from the second gate and the last diode of
8 the plurality of serially connected diodes to the power supply
9 connection;

10 wherein an ESD event causes a current to flow through said plurality of
11 serially connected diodes and said second resistor to trigger the
12 shallow trench isolation bounded SCR to turn on.

1 59. The ESD protection circuit of claim 53 wherein said biasing circuit: comprises:

2 a resistor/capacitor biasing circuit comprising:

3 a first resistor connected from the signal input/output interface to
4 the first gate of said shallow trench isolation bounded SCR,
5 and

6 a first capacitor connected from the first gate of the shallow
7 trench isolation bounded SCR to said power supply
8 connection,

9 wherein upon said ESD event, a top plate of said capacitor
10 connected to said gate of the shallow trench isolation
11 bounded is virtually connected to said power supply
12 connection and said shallow trench isolation bounded SCR
13 is activated;

14 a diode triggering biasing circuit comprising:

15 a plurality of serially connected diodes, where a first diode of said
16 plurality of serially connected diodes is connected to the signal
17 input/output interface and a last diode of said plurality of serially
18 connected diodes is connected to a second gate of said shallow
19 trench isolation bounded SCR, and

20 a second resistor connected from the second gate and the last diode of
21 the plurality of serially connected diodes to the power supply
22 connection,

23 wherein an ESD event causes a current to flow through said plurality of
24 serially connected diodes and said second resistor to trigger the
25 shallow trench isolation bounded SCR to turn on.

1 60. A method for forming an ESD protection circuit formed at an input/output
2 interface of an integrated circuit formed on a substrate to protect said integrated
3 circuit from damage caused by an ESD event, said ESD protection circuit
4 comprising:

5 forming a shallow trench isolation bounded SCR on a surface of said
6 substrate;

7 connecting said shallow trench isolation bounded SCR between a signal
8 input/output interface of said integrated circuit and a power supply
9 connection of said integrated circuit;

10 forming a biasing circuit; and

11 connecting said biasing circuit to said shallow trench isolation bounded
12 SCR to bias said shallow trench isolation bounded SCR to turn on
13 more rapidly during said ESD event.

1 61. The method of claim 60 further comprising the steps of:

2 forming at least one diode on said substrate; and

3 connecting said diode between said signal input/output interface and an
4 anode connection of said shallow trench isolation bounded SCR to
5 increase a holding voltage for said shallow trench isolation bounded
6 SCR when said shallow trench isolation bounded SCR is turned on.

1 62. The method of claim 60 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a shallow trench isolation bounded diode said shallow trench
4 isolation bounded diode; and
5 connecting said shallow trench isolation bounded diode to the signal
6 input/output interface,

1 63. The method of claim 62 wherein forming said biasing circuit further comprises the
2 steps of:

3 forming a second resistance of the material of the second well from said
4 first gate to said first diffusion region.

1 64. The method of claim 60 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a first resistor from the signal input/output interface to the first
4 gate of said shallow trench isolation bounded SCR; and

5 forming a first capacitor from the first gate of the shallow trench
6 isolation bounded SCR to said power supply connection;
7 wherein upon said ESD event, a top plate of said capacitor connected
8 to said gate of the shallow trench isolation bounded virtually
9 connected to said power supply connection and said shallow trench
10 isolation bounded SCR is activated.

1 65. The method of claim 60 wherein said biasing circuit: comprises the steps of:
2 forming a plurality of serially connected diodes;
3 connecting a first diode of said plurality of serially connected diodes to the
4 signal input/output interface;
5 connecting a last diode of said plurality of serially connected diodes to a
6 second gate of said shallow trench isolation bounded SCR; and
7 forming a second resistor from the second gate and the last diode of the
8 plurality of serially connected diodes to the power supply connection;
9 wherein an ESD event causes a current to flow through said plurality of
10 serially connected diodes and said second resistor to trigger the
11 shallow trench isolation bounded SCR to turn on.

1 66. The method of claim 60 wherein forming said biasing circuit: comprises the steps
2 of:

3 forming a resistor/capacitor biasing circuit by the steps of:

4 forming a first resistor from the signal input/output interface to
5 the first gate of said shallow trench isolation bounded SCR,
6 and

7 forming a first capacitor from the first gate of the shallow trench
8 isolation bounded SCR to said power supply connection,

9 wherein upon said ESD event, a top plate of said capacitor
10 connected to said gate of the shallow trench isolation
11 bounded virtually connected to said power supply connection
12 and said shallow trench isolation bounded SCR is activated.

13 forming a diode triggering biasing circuit by the steps of:

14 forming a plurality of serially connected diodes;

15 connecting a first diode of said plurality of serially connected diodes to
16 the signal input/output interface,

17 connecting a last diode of said plurality of serially connected diodes to
18 a second gate of said shallow trench isolation bounded SCR, and

19 forming a second resistor from the second gate and the last diode of
20 the plurality of serially connected diodes to the power supply
21 connection,

22 wherein an ESD event causes a current to flow through said plurality of
23 serially connected diodes and said second resistor to trigger the
24 shallow trench isolation bounded SCR to turn on.